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09/544,822

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April 6, 2000

First Named Inventor

Tongbi Jiang

Art Unit

2822

Examiner Name

D. Graybill

Attorney Docket Number

2269-4241US (99-0408.00/US)

ENCLOSURES (check all that apply)☐ Fee Transmittal Form☐ Fee Attached☐ Amendment / Reply☐ After Final☐ Affidavits/declaration(s)☐ Extension of Time Request☐ Express Abandonment Request☐ Information Disclosure Statement☐ Certified Copy of Priority Document(s)☐ Reply to Missing Parts/
Incomplete Application☐ Reply to Missing Parts
under 37 CFR 1.52 or 1.53☐ Drawing(s)☐ Licensing-related Papers☐ Petition☐ Petition to Convert to a
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the amount of \$500.00☐ Proprietary Information☐ Status Letter☒ Other Enclosure(s)
(please identify below):APPENDIX A - Claims Appendix - Claims
1-5, 7-32 and 58-64 - U.S. Patent
Application No. 09/544,822 Filed April 6,
2000**Remarks**The Commissioner is authorized to charge any additional fees required but not submitted
with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to
Deposit Account 20-1469 during pendency of this application.**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm

TraskBritt, P.C.

Signature

Printed Name

James R. Duzan

Date

February 14, 2007

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No.

28,393

CERTIFICATE OF MAILINGExpress Mail Label Number: EV827469925USDate of Deposit: February 14, 2007Person Making Deposit: Sharley Thayne

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tongbi Jiang

Serial No.: 09/544,822

Filed: April 6, 2000

For: UNDERFILL PROCESS

Confirmation No.: 9308

Examiner: D. Graybill

Group Art Unit: 2822

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BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is submitted as a single copy pursuant to 37 C.F.R. § 41.37 and in the format required by 37 C.F.R. § 41.37(c) (1).

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1) REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., a corporation of the State of Delaware, having a place of business at 8000 South Federal Way, Boise, Idaho 83707-006, Reel/Frame 10723/0869.

2) RELATED APPEALS AND INTERFERENCES

Neither Appellants, the Appellants' representative, nor the Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

3) STATUS OF THE CLAIMS

Claims 1 through 5 and 7 through 64 are currently pending in the application.

Claim 6 was previously canceled.

Claims 33 through 57 are withdrawn from consideration.

Claims 1 through 5, 7 through 32 and 58 through 64 stand rejected.

No claims are allowed

The rejection of claims 1 through 5, 7 through 32 and 58 through 64 is being appealed.

4) STATUS OF AMENDMENTS

No proposed amendments were submitted after the current final rejection.

5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Initially set forth below by Appellant in compliance with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject mater of each independent claim being appealed identified by the appropriate line and page of the specification as well as drawing figure is a summary and map for appealed independent claims 1, 10, 58, 62, and 64 and dependent claims 13, 14, 16-21, 21-32 and 61.

Summary and Map for Appealed Independent claim 1

To comply with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject mater of each independent claim being appealed identified by the appropriate line and page of the specification as well as drawing figure, referring to drawing FIGs. 1-15 and referring to independent claim 1, the present invention is directed to [a] method of applying a material 28 between a semiconductor device 12 having a surface 20 and substrate 10 having a surface 18, said method comprising:

applying a liquid wetting agent layer 2 to one of said surface 18, 20 of said semiconductor device 12 and said surface of said substrate 10; (Specification, page 5, lines 5-14, p. 10, lines 1-20) and

applying a flowable underfill material 28 between the substrate 10 and the semiconductor device 12, such that said flowable material 28 contacts said liquid wetting agent layer 2. (Specification, page 5, lines 5-14, p. 10, line 21- page 11, line 5).

Summary and Map for Appealed Independent claim 10

To comply with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject mater of each independent claim being appealed identified by the appropriate line and page of the specification as well as drawing figure, referring to drawing FIGs. 1-15 and referring to independent claim 10, the present invention is directed to [a] method of applying a material 28 between a semiconductor device 12 having a surface 20 and substrate 10 having a surface 18, said method comprising:

providing a semiconductor device 12 having an active surface 20, another surface, a first end 30, a second end 30', a first lateral side 32, and a second lateral side 32', said first end 30, said second end 30', said first lateral side 32, and said second lateral side 32' forming at least a portion of a periphery of said semiconductor device 12; (Specification, page 9, lines 1-5)

providing a substrate 10 having an upper surface 18, a first side wall 14, a second side wall 14', a first lateral side wall 16 and a second lateral side wall 16'; (Specification, page 8, lines 20-27)

applying a liquid wetting agent layer 2 to one of said active surface 20 of said semiconductor device 12 and said upper surface 18 of said substrate 10; (Specification, page 10, lines 1-4) and

applying a flowable underfill material 28 between said semiconductor device 12 and said substrate 10, such that said flowable material 28 contacts said applied liquid wetting agent layer 2. (Specification, page 10, line 21 – page 11, line 5)

Summary and Map for Appealed Dependent claims 13, 14, 16-21 and 23-32

To comply with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject matter of each of dependent claims 13, 14, 16-21 and 23-32 identified by the appropriate line and page of the specification as well as drawing figure.

13. The method according to claim 10, wherein said substrate 10 includes an aperture 38 extending through said substrate 10. (FIG. 5, Specification, page 13, lines 1-9).

14. The method according to claim 13, wherein said aperture 38 is located adjacent to said another surface of said semiconductor device 12. (FIG. 5, Specification, page 13, lines 1-9).

16. The method according to claim 10, further comprising: elevating at least said first side wall 14 of said substrate 10 and said first end 30 of said semiconductor device 12. (FIGs. 7-9, Specification, page 13, line 10 – page 14, line 9).

17. The method according to claim 16, wherein said elevating said first side wall 14 of said substrate 10 comprises placing said substrate 10 on a support structure 44 and elevating at

least one portion of said support structure 44. (FIGs. 7-9, Specification, page 13, line 10 – page 15, line 14).

18. The method according to claim 16, further comprising: providing a dam 40 on the substrate 10 adjacent to at least one of said first end 30, said second end 30', said first lateral side 16 and said second lateral side 16' of said semiconductor device 12. (FIGs. 7-9, Specification, page 14, line 10 – page 15, line 7).

19. The method according to claim 18, wherein said dam 40 extends to substantially between said semiconductor device 12 and said substrate 10. (FIGs. 7-9, Specification, page 13, line 10 – page 15, line 14).

20. The method of claim 10, further comprising: vibrating one of said semiconductor device 12 and said substrate 10. (FIGs. 7-9, Specification, page 15, lines 15-19).

21. The method according to claim 20, wherein said vibrating one of said semiconductor device and said substrate 10 comprises placing said substrate 10 on a support structure 44 and vibrating said support structure 44. (FIGs. 7-9, Specification, page 15, lines 15-19).

23. The method according to claim 10, wherein said substrate 10 includes at least one aperture 70 extending through said substrate 10 and substantially located adjacent to said another surface of said semiconductor device 12. (FIG. 11, Specification, page 16, lines 13-22).

24. The method according to claim 23, wherein said flowable material 28 is provided through said at least one aperture 70 of said substrate 10 substantially filling a gap between said substrate 10 and said semiconductor device 12. (FIG. 11, Specification, page 16, lines 13-22).

25. The method according to claim 18, wherein said applying said flowable material 28 comprises: providing said flowable material 28 substantially adjacent to said first end 30 of

said semiconductor device 12 for filling a gap between said substrate 10 and said semiconductor device 12. (FIG. 3, Specification, page 12, lines 16-26).

26. The method according to claim 18, wherein said applying said flowable material 28 comprises: providing said flowable material 28 substantially adjacent to said first end 30 and one of said first lateral side 32 and said second lateral side 32' of said semiconductor device 12 for filling a gap between said substrate 10 and said semiconductor device 12. (FIG. 3, Specification, page 12, lines 16-26).

27. The method according to claim 18, wherein said substrate 10 includes at least one aperture 70 extending therethrough and substantially located adjacent to said another surface of said semiconductor device 12. (FIG. 11, Specification, page 16, lines 13-22).

28. The method according to claim 27, wherein said flowable material 28 is provided through said at least one aperture 70. (FIG. 11, Specification, page 16, lines 13-22).

29. The method according to claim 28, wherein said flowable material 28 is provided from below said substrate 10. (FIG. 13, Specification, page 17, lines 5-19).

30. The method according to claim 28, wherein said flowable material 28 is provided through said at least one aperture 70 contacting at least a portion of said another surface of said semiconductor device 12. (FIGs. 11-13, Specification, page 16, line 13- page 17, line 19).

31. The method according to claim 10, wherein said applying said flowable material 28 between said semiconductor device 12 and said substrate 10 further comprises placing said semiconductor device 12 and said substrate 10 in a chamber, said chamber having an atmosphere therein having a variable pressure. (FIGs. 14, 15, Specification, page 16, lines 4-13).

32. The method according to claim 31, further comprising: varying the pressure of said atmosphere in said chamber for said flowable material 28 substantially filling a gap between

said semiconductor device 12 and said substrate 10. (FIGs. 14, 15, Specification, page 16, lines 4-13).

Summary and Map for Appealed Independent claim 58 and dependent claim 61

To comply with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject matter of each independent claim being appealed identified by the appropriate line and page of the specification as well as drawing figure, referring to drawing FIGs. 1-15 and referring to independent claim 58, the present invention is directed to [a] method for attaching a semiconductor assembly, said method comprising:

providing a semiconductor device 12 having an active surface (Specification, page 9, lines 1-5);
providing a substrate 10 having an upper surface (Specification, page 8, lines 20-27);
applying a liquid wetting agent layer 2 to one of said active surface of said semiconductor device 12 and said upper surface of said substrate 10 (Specification, page 10, lines 1-4);
connecting said semiconductor device 12 to said substrate 10 so that said active surface of said semiconductor device 12 faces said upper surface of said substrate 10 (Specification, page 9, lines 6-20); and
applying a flowable underfill material 28 between the substrate 10 and the semiconductor device 12, such that said flowable underfill material 28 contacts said applied wetting agent layer 2. (Specification, page 10, line 21 – page 11, line 5)

Claim 61, which depends from claim 58, further recites the “wetting agent layer 2 comprises a silane-based material” and finds support, at least, at Specification, page 9, lines 1-5.

Summary and Map for Appealed Independent claim 62

To comply with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject matter of each independent claim being appealed identified by the appropriate line and page of the specification as well as drawing figure, referring to drawing FIGs. 1-15 and

referring to independent claim 62, the present invention is directed to [a] method for attaching a semiconductor assembly, said method comprising:

providing a semiconductor device 12 having an active surface, a first end, a second end, a first lateral side end and a second lateral side end (Specification, page 9, lines 1-5);

providing a substrate 10 having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall (Specification, page 8, lines 20-25);

applying a silane-based material layer to one of a portion of said active surface of said semiconductor device 12 and a portion of said upper surface of said substrate 10 (Specification, page 10, lines 1-20);

connecting said semiconductor device 12 to said substrate 10 so that said active surface of said semiconductor device 12 faces said upper surface of said substrate 10 (Specification, page 9, lines 6-20); and

applying a flowable underfill material 28 between said semiconductor device 12 and said substrate 10, such that said flowable underfill material 28 contacts said applied silane-based material layer. (Specification, page 10, line 21 – page 11, line 5)

Summary and Map for Appealed Independent claim 64

To comply with the provisions of 37 CFR § 1.41.37 to provide a summary and map of the claimed subject matter of each independent claim being appealed identified by the appropriate line and page of the specification as well as drawing figure, referring to drawing FIGs. 1-15 and referring to independent claim 64, the present invention is directed to [a] method of applying a material 28 between a semiconductor device 12 having a surface 18 and substrate 10 having a surface 20, said method comprising:

applying a essentially uniform liquid silane-based wetting agent layer 2 having a total thickness of about a monolayer to at least one of said surface of said semiconductor device 12 and said surface of said substrate 10 (Specification, page 10, lines 1-20); and

applying a flowable underfill material 28 between the substrate 10 and the semiconductor device 12 separately from said liquid silane-based wetting agent layer 2, such that said flowable material 28 contacts said wetting agent layer 2. (Specification, page 10, line 21 – page 11, line 5)

6) GROUND OF REJECTION TO BE REVIEWED

A. Whether claims 58-61 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Yamada (U.S. Patent 5,959,363).

B. Whether claims 1-5, 7-12, 22, 62, 63 and 64 are unpatentable under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz (U.S. Patent 6,350,840) and Pluddemann (U.S. Patent 4,961,967).

C. Whether claim 64 is unpatentable under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz (U.S. Patent 6,350,840) and Pluddemann (U.S. Patent 4,961,967), in further combination with Hieda (U.S. Patent 6,303,277).

D. Whether claims 13, 14, 16-21 and 23-30 are unpatentable under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz (U.S. Patent 6,350,840) and Pluddemann (U.S. Patent 4,961,967) and in further combination with Akram (U.S. Patent 5,766,982).

E. Whether claims 31 and 32 are unpatentable under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz and Pluddemann as applied to claim 10, and in further combination with Banerji (U.S. Patent 5,203,076).

7) ARGUMENT

(i) 35 U.S.C. § 102(e)

Appellant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 58-61 stand rejected under 35 U.S.C. §102(e) as being anticipated by Yamada (U.S. Patent 5,959,363).

a. Claims 58-60

Claim 58 recites “[a] method for attaching a semiconductor assembly, said method comprising: providing a semiconductor device having an active surface; providing a substrate having an upper surface; applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and applying a flowable underfill material between the substrate and the semiconductor device, such that said flowable underfill material contacts said applied wetting agent layer.”

Yamada describes a semiconductor device comprising a wiring circuit board 202 and a semiconductor chip 201 mounted through a bump electrode 203 on the circuit board 202, a space between the circuit board 202 and the semiconductor chip 201 as well as a periphery of the semiconductor chip 201 being encapsulated with a resin containing a filler. A passivation film of the semiconductor chip 201 is formed of a polymer film, such as a hydrocarbon wax, a fatty acid type wax, a fatty amide type wax or an ester type wax or resin layer. (Yamada, col. 56, line 24 – col. 57, line 20).

Appellant asserts that the Yamada et al. reference does not anticipate the presently claimed invention of independent claim 58 because the Yamada et al. reference does not identically describe each and every element as set forth in the claim, either expressly or inherently described, in as complete detail as is contained in the claim. Appellant asserts that the Yamada et al. reference does not identically describe, either expressly or inherently, the elements

of the presently claimed invention of independent claim 58 calling for “applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate” and “applying a flowable underfill material between the substrate and the semiconductor device, such that said flowable underfill material contacts said applied wetting agent layer.”

In contrast to the elements of the presently claimed invention of independent claim 58, the Yamada et al. reference describes the use of a wax layer. Appellant asserts that the Yamada et al. wax layer is not a “liquid wetting agent layer” as recited in claim 58 and does not describe applying a wetting agent or essentially uniform liquid silane-based wetting agent layer having a thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate whatsoever. Further, the Examiner admits that Yamada does not explicitly disclose that “said flowable [underfill] material contacts said [applied] wetting agent layer.” (October 20, 2006, Office Action, page 9-10). Therefore, Yamada et al. al. does not anticipate independent claim 58. Accordingly, independent claim 58 is allowable as well as the dependent claims 59 through 60 therefrom. Thus, the rejection of independent claim 58, and dependent claims 59-60 therefrom, should be reversed.

b. Claim 61

Claim 61 depends from claim 58 and is allowable at least for each of the reasons stated with respect to claim 58. The arguments with respect to claim 58 are incorporated herein. Claim 61 is further allowable as Yamada fails to describe, either expressly or inherently, that the wetting agent comprises a silane-based material. *See*, October 20, 2006, Office Action, page 9-10.

(ii) 35 U.S.C. § 103(a)

With respect to the rejections under 35 U.S.C. §103(a), M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

- a. Claims 1-5, 7-12, 22, 62 and 64 stand rejected under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz (U.S. Patent 6,350,840) and Pluddemann (U.S. Patent 4,961,967).

Turning to the cited prior art, the Yamada et al. reference teaches or suggests a semiconductor device comprising a wiring circuit board 202 and a semiconductor chip 201 mounted through a bump electrode 203 on the circuit board 202, a space between the circuit board 202 and the semiconductor chip 201 as well as a periphery of the semiconductor chip being encapsulated with a resin containing a filler. (Yamada, col. 54, lines 1-7) A passivation film of the semiconductor chip 201 is formed of a polymer film, such as a hydrocarbon wax, a fatty acid type wax, a fatty amide type wax or an ester type wax or resin layer. (Yamada, col. 54, lines 30-33). The Yamada et al. reference solely teaches or suggests that "[t]he encapsulation resin should preferably be a thermosetting resin of non-solvent type in general, but the resin is not limited to a bisphenol type epoxy resin." (Yamada, col. 70, lines 8-15, col. 55, line 58- col. 56, line 5). Also, the Yamada et al. reference teaches or suggests that the resin comprises a first resin and a second resin. A first resin and a second resin does not teach or suggest any resin but a thermosetting resin, the sole type of resin in the Yamada et al. specification.

The Schultz reference teaches or suggests the use of a thermoplastic material for an encapsulant.

The Pluddemann reference is cited for teaching that the flowable material contacts the liquid wetting agent layer and that the liquid wetting agent is silane-based. (October 20, 2006, Office Action, page 9). The Pluddemann reference teaches or suggests a primer composition for improving adhesion between a solid substrate and a thermo-plastic resin. The composition consists essentially of 1 to 25 weight percent of an organosilicon compound selected from a group of silane compounds or partial hydrolyzates thereof and 75 to 99 weight percent of an alkoxymethyltriazine. (Pluddemann, col. 1, lines 55-64). The primer compound of Pluddemann is not directed to an improved flow of an underfill material that is a thermo-setting material.

i. Claims 1-5 and 7-9

Claim 1 of the presently claimed invention recites “[a] method for applying a material between a semiconductor device having a surface and a substrate having a surface, said method comprising: applying a liquid wetting agent layer to one of said surface of said semiconductor device and said surface of said substrate; and applying a flowable underfill material between the substrate and the semiconductor device, such that said flowable material contacts said liquid wetting agent layer.”

Appellant asserts that any combination of the Yamada et al. reference, the Schulz et al. reference, and the Pluddemann reference fails to teach or suggest the claim limitations of independent claim 1 and dependent claims 2-5 and 7-9 therefrom. Specifically, Yamada et al., Schulz et al. reference, and Pluddemann fail to teach or suggest “applying a liquid wetting agent layer to one of said surface of said semiconductor device and said surface of said substrate” or “applying a flowable underfill material between the substrate and the semiconductor device, such that said flowable material contacts said liquid wetting agent layer” as recited in claim 1.

Appellant asserts that the Yamada et al. reference clearly uses a thermo-setting material as an underfill material because the Yamada teaches or suggests thermo-setting resin. (Yamada, col. 56, lines, 23-61). Contrary to the Examiner’s assertion, Yamada does not teach that the “underfill material is not limited to thermosetting material,” but rather that the “resin is not limited to bisphenol type epoxy resin.” (Cf., October 20, 2006, Office Action, page 9 and Yamada col. 70, lines 8-14 and 62).

Appellant further asserts that the Yamada et al. reference cannot teach or suggest the use of a thermo-plastic underfill because a thermo-plastic underfill would soften with an increase of temperature when the IC chip is being operated so that the thermo-plastic underfill would be unable to compensate for any thermal mismatch between IC chip and the IC carrier thereby making the Yamada et al. invention inoperable due to the thermo-plastic material losing its strength as it is heated thereby allowing the IC chip to separate from the substrate as the bump electrodes 203 fail in shear due to the thermo-plastic material carrying no load. Additionally, thermo-plastic materials have too high viscosity to be used as underfill materials as they are unable to effectively fill the small space between an IC chip mounted on an IC chip carrier using solder balls where the small space is 125 microns or less in height.

The Examiner cites the Schultz reference for teaching the use of a thermoplastic underfill material. (October 20, 2006, Office Action, page 9). Appellant asserts that the Schultz reference solely teaches or suggests the use of a thermoplastic material for an encapsulant.

Appellant asserts that both the Schulz et al. reference and the Pluddemann reference teaches away from any combination with and modification of the Yamada et al. reference. Yet further, Appellant asserts that one of ordinary skill in the art would not substitute the use of a thermo-plastic for the thermo-setting underfill of Yamada et al. Appellant asserts the one of ordinary skill in the art would not substitute either the thermo-plastic resin of the Schultz et al. reference or the liquid primer composition from the Pluddemann reference to be separately applied to the IC chip and/or IC carrier of the Yamada et al. reference. The substitution of a thermo-plastic resin of Schultz et al. for a thermo-setting resin of Yamada et al. destroys the Yamada et al. invention as it would fail since in operation, the thermoplastic resin of Schultz et al. would allow the device to separate and the bump electrodes 203 to fail in shear due to the thermo-plastic resin carrying no load. Further, Appellant asserts that the substitution of a liquid primer composition from the Pluddemann reference for a resin of the Yamada et al. reference cannot be the substitution of an equivalent. Appellant asserts that one of ordinary skill in the art would not use the Pluddemann liquid primer composition for use with thermo-setting plastics of Yamada et al.

Appellant asserts that the sole teaching or suggestion for the use of a liquid wetting agent on one of the active surface of said semiconductor device and a portion of said upper surface of

said substrate for use with an underfill material is solely the Appellant's disclosure because the cited prior art teaches away from any combination thereof, because if the prior art is combined as suggested in the rejection, the combination clearly destroys the operability of the primary reference and because the cited prior art does not contain any suggestion for any combination thereof. Solely Appellant's disclosure contains any such suggestion as evidenced by the attempt to combine the cited prior art in a rejection which destroys the invention of the Yamada et al. reference.

Therefore, Appellant asserts that any combination of the Yamada et al. reference, the Schultz et al. reference, and the Pluddemann reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 1 as well as the dependent claims therefrom. Accordingly, the rejection of independent claim 1 as well as dependent claims 2-5 and 7-9 therefrom should be reversed.

ii. Claims 10-12, 22

Claim 10 of the presently claimed invention "[a] method for applying a material between a semiconductor device and a substrate, said method comprising: providing a semiconductor device having an active surface, another surface, a first end, a second end, a first lateral side, and a second lateral side, said first end, said second end, said first lateral side, and said second lateral side forming at least a portion of a periphery of said semiconductor device; providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; and applying a flowable underfill material between said semiconductor device and said substrate, such that said flowable material contacts said applied liquid wetting agent layer."

Appellant asserts that any combination of the Yamada et al. reference, the Schulz et al. reference, and the Pluddemann reference fails to teach or suggest the claim limitations of independent claim 10 and dependent claims 11, 12 and 22 therefrom. Specifically, Yamada et al., Schulz et al. reference, and Pluddemann fail to teach or suggest "applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate" or "applying a flowable underfill material between said semiconductor device and

said substrate, such that said flowable material contacts said applied liquid wetting agent layer” as recited in claim 10.

Appellant asserts that the Yamada et al. reference clearly uses a thermo-setting material as an underfill material because the Yamada teaches or suggests thermo-setting resin. (Yamada, col. 56, lines, 23-61). Contrary to the Examiner’s assertion, Yamada does not teach that the “underfill material is not limited to thermosetting material,” but rather that the “resin is not limited to bisphenol type epoxy resin.” (Cf., October 20, 2006, Office Action, page 9 and Yamada col. 70, lines 8-14 and 62).

Appellant further asserts that the Yamada et al. reference cannot teach or suggest the use of a thermo-plastic underfill because a thermo-plastic underfill would soften with an increase of temperature when the IC chip is being operated so that the thermo-plastic underfill would be unable to compensate for any thermal mismatch between IC chip and the IC carrier thereby making the Yamada et al. invention inoperable due to the thermo-plastic material losing its strength as it is heated thereby allowing the IC chip to separate from the substrate as the bump electrodes 203 fail in shear due to the thermo-plastic material carrying no load. Additionally, thermo-plastic materials have too high viscosity to be used as underfill materials as they are unable to effectively fill the small space between an IC chip mounted on an IC chip carrier using solder balls where the small space is 125 microns or less in height.

The Examiner cites the Schultz reference for teaching the use of a thermoplastic underfill material. (October 20, 2006, Office Action, page 9). Appellant asserts that the Schultz reference solely teaches or suggests the use of a thermoplastic material for an encapsulant.

Appellant asserts that both the Schulz et al. reference and the Pluddemann reference teaches away from any combination with and modification of the Yamada et al. reference. Yet further, Appellant asserts that one of ordinary skill in the art would not substitute the use of a thermo-plastic for the thermo-setting underfill of Yamada et al. Appellant asserts the one of ordinary skill in the art would not substitute either the thermo-plastic resin of the Schultz et al. reference or the liquid primer composition from the Pluddemann reference to be separately applied to the IC chip and/or IC carrier of the Yamada et al. reference. The substitution of a thermo-plastic resin of Schultz et al. for a thermo-setting resin of Yamada et al. destroys the Yamada et al. invention as it would fail since in operation, the thermoplastic resin of Schultz et

al. would allow the device to separate and the bump electrodes 203 to fail in shear due to the thermo-plastic resin carrying no load. Further, Appellant asserts that the substitution of a liquid primer composition from the Pluddemann reference for a resin of the Yamada et al. reference cannot be the substitution of an equivalent. Appellant asserts that one of ordinary skill in the art would not use the Pluddemann liquid primer composition for use with thermo-setting plastics of Yamada et al.

Appellant asserts that the sole teaching or suggestion for the use of a liquid wetting agent on one of the active surface of said semiconductor device and a portion of said upper surface of said substrate for use with an underfill material is solely the Appellant's disclosure because the cited prior art teaches away from any combination thereof, because if the prior art is combined as suggested in the rejection, the combination clearly destroys the operability of the primary reference and because the cited prior art does not contain any suggestion for any combination thereof. Solely Appellant's disclosure contains any such suggestion as evidenced by the attempt to combine the cited prior art in a rejection which destroys the invention of the Yamada et al. reference.

Therefore, Appellant asserts that any combination of the Yamada et al. reference, the Schultz et al. reference, and the Pluddemann reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 10 as well as the dependent claims therefrom. Accordingly, the rejection of independent claim 10 as well as dependent claims 11, 12 and 22 therefrom should be reversed.

iii. Claims 62 and 63

Claim 62 of the presently claimed invention recites "[a] method for attaching a semiconductor assembly, said method comprising: providing a semiconductor device having an active surface, a first end, a second end, a first lateral side end and a second lateral side end; providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; applying a silane-based material layer to one of a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate; connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and applying a flowable

underfill material between said semiconductor device and said substrate, such that said flowable underfill material contacts said applied silane-based material layer.”

Appellant asserts that any combination of the Yamada et al. reference, the Schulz et al. reference, and the Pluddemann reference fails to teach or suggest the claim limitations of independent claim 62. Specifically, Yamada et al., Schulz et al. reference, and Pluddemann fail to teach or suggest “applying a silane-based material layer to one of a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate” or “applying a flowable underfill material between said semiconductor device and said substrate, such that said flowable underfill material contacts said applied silane-based material layer” as recited in claim 62.

Appellant asserts that the Yamada et al. reference clearly uses a thermo-setting material as an underfill material because the Yamada teaches or suggests thermo-setting resin. (Yamada, col. 56, lines, 23-61). Contrary to the Examiner’s assertion, Yamada does not teach that the “underfill material is not limited to thermosetting material,” but rather that the “resin is not limited to bisphenol type epoxy resin.” (Cf., October 20, 2006, Office Action, page 9 and Yamada col. 70, lines 8-14 and 62).

Appellant further asserts that the Yamada et al. reference cannot teach or suggest the use of a thermo-plastic underfill because a thermo-plastic underfill would soften with an increase of temperature when the IC chip is being operated so that the thermo-plastic underfill would be unable to compensate for any thermal mismatch between IC chip and the IC carrier thereby making the Yamada et al. invention inoperable due to the thermo-plastic material losing its strength as it is heated thereby allowing the IC chip to separate from the substrate as the bump electrodes 203 fail in shear due to the thermo-plastic material carrying no load. Additionally, thermo-plastic materials have too high viscosity to be used as underfill materials as they are unable to effectively fill the small space between an IC chip mounted on an IC chip carrier using solder balls where the small space is 125 microns or less in height.

The Examiner cites the Schultz reference for teaching the use of a thermoplastic underfill material. (October 20, 2006, Office Action, page 9). Appellant asserts that the Schultz reference solely teaches or suggests the use of a thermoplastic material for an encapsulant.

Appellant asserts that both the Schulz et al. reference and the Pluddemann reference teaches away from any combination with and modification of the Yamada et al. reference. Yet further, Appellant asserts that one of ordinary skill in the art would not substitute the use of a thermo-plastic for the thermo-setting underfill of Yamada et al. Appellant asserts the one of ordinary skill in the art would not substitute either the thermo-plastic resin of the Schultz et al. reference or the liquid primer composition from the Pluddemann reference to be separately applied to the IC chip and/or IC carrier of the Yamada et al. reference. The substitution of a thermo-plastic resin of Schultz et al. for a thermo-setting resin of Yamada et al. destroys the Yamada et al. invention as it would fail since in operation, the thermoplastic resin of Schultz et al. would allow the device to separate and the bump electrodes 203 to fail in shear due to the thermo-plastic resin carrying no load. Further, Appellant asserts that the substitution of a liquid primer composition from the Pluddemann reference for a resin of the Yamada et al. reference cannot be the substitution of an equivalent. Appellant asserts that one of ordinary skill in the art would not use the Pluddemann liquid primer composition for use with thermo-setting plastics of Yamada et al.

Appellant asserts that the sole teaching or suggestion for the use of a liquid wetting agent on one of the active surface of said semiconductor device and a portion of said upper surface of said substrate for use with an underfill material is solely the Appellant's disclosure because the cited prior art teaches away from any combination thereof, because if the prior art is combined as suggested in the rejection, the combination clearly destroys the operability of the primary reference and because the cited prior art does not contain any suggestion for any combination thereof. Solely Appellant's disclosure contains any such suggestion as evidenced by the attempt to combine the cited prior art in a rejection which destroys the invention of the Yamada et al. reference.

Therefore, Appellant asserts that any combination of the Yamada et al. reference, the Schultz et al. reference, and the Pluddemann reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 62 and dependent claim 63 therefrom. Accordingly, the rejection of independent claim 62 and dependent claim 63 should be reversed.

iv. Claim 64

Claim 64 of the presently claimed invention recites “[a] method for applying a material between a semiconductor device having a surface and a substrate having a surface, said semiconductor device mounted on said substrate, said method comprising: applying a essentially uniform liquid silane-based wetting agent layer having a total thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate; and applying a flowable underfill material between the substrate and the semiconductor device separately from said liquid silane-based wetting agent layer, such that said flowable material contacts said wetting agent layer.”

Appellant asserts that any combination of the Yamada et al. reference, the Schulz et al. reference, and the Pluddemann reference fails to teach or suggest the claim limitations of independent claim 64. Specifically, Yamada et al., Schulz et al. reference, and Pluddemann fail to teach or suggest “applying a essentially uniform liquid silane-based wetting agent layer having a total thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate” or “applying a flowable underfill material between the substrate and the semiconductor device separately from said liquid silane-based wetting agent layer, such that said flowable material contacts said wetting agent layer” as recited in claim 64.

Appellant asserts that the Yamada et al. reference clearly uses a thermo-setting material as an underfill material because the Yamada teaches or suggests thermo-setting resin. (Yamada, col. 56, lines, 23-61). Contrary to the Examiner’s assertion, Yamada does not teach that the “underfill material is not limited to thermosetting material,” but rather that the “resin is not limited to bisphenol type epoxy resin.” (Cf., October 20, 2006, Office Action, page 9 and Yamada col. 70, lines 8-14 and 62).

Appellant further asserts that the Yamada et al. reference cannot teach or suggest the use of a thermo-plastic underfill because a thermo-plastic underfill would soften with an increase of temperature when the IC chip is being operated so that the thermo-plastic underfill would be unable to compensate for any thermal mismatch between IC chip and the IC carrier thereby making the Yamada et al. invention inoperable due to the thermo-plastic material loosing its strength as it is heated thereby allowing the IC chip to separate from the substrate as the bump electrodes 203 fail in shear due to the thermo-plastic material carrying no load. Additionally, thermo-plastic materials have too high viscosity to be used as underfill materials as they are

unable to effectively fill the small space between an IC chip mounted on an IC chip carrier using solder balls where the small space is 125 microns or less in height.

The Examiner cites the Schultz reference for teaching the use of a thermoplastic underfill material. (October 20, 2006, Office Action, page 9). Appellant asserts that the Schultz reference solely teaches or suggests the use of a thermoplastic material for an encapsulant.

Appellant asserts that both the Schulz et al. reference and the Pluddemann reference teaches away from any combination with and modification of the Yamada et al. reference. Yet further, Appellant asserts that one of ordinary skill in the art would not substitute the use of a thermo-plastic for the thermo-setting underfill of Yamada et al. Appellant asserts the one of ordinary skill in the art would not substitute either the thermo-plastic resin of the Schultz et al. reference or the liquid primer composition from the Pluddemann reference to be separately applied to the IC chip and/or IC carrier of the Yamada et al. reference. The substitution of a thermo-plastic resin of Schultz et al. for a thermo-setting resin of Yamada et al. destroys the Yamada et al. invention as it would fail since in operation, the thermoplastic resin of Schultz et al. would allow the device to separate and the bump electrodes 203 to fail in shear due to the thermo-plastic resin carrying no load. Further, Appellant asserts that the substitution of a liquid primer composition from the Pluddemann reference for a resin of the Yamada et al. reference cannot be the substitution of an equivalent. Appellant asserts that one of ordinary skill in the art would not use the Pluddemann liquid primer composition for use with thermo-setting plastics of Yamada et al.

Appellant asserts that the sole teaching or suggestion for the use of a liquid wetting agent on one of the active surface of said semiconductor device and a portion of said upper surface of said substrate for use with an underfill material is solely the Appellant's disclosure because the cited prior art teaches away from any combination thereof, because if the prior art is combined as suggested in the rejection, the combination clearly destroys the operability of the primary reference and because the cited prior art does not contain any suggestion for any combination thereof. Solely Appellant's disclosure contains any such suggestion as evidenced by the attempt to combine the cited prior art in a rejection which destroys the invention of the Yamada et al. reference.

Therefore, Appellant asserts that any combination of the Yamada et al. reference, the Schultz et al. reference, and the Pluddemann reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 64. Accordingly, the rejection of independent claim 64 should be reversed.

- b. Claim 64 stands rejected under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz (U.S. Patent 6,350,840) and Pluddemann (U.S. Patent 4,961,967), in further combination with Hieda (U.S. Patent 6,303,277).

The discussion of Yamada, Schultz and Pluddemann, *supra*, is incorporated herein. The Hieda reference teaches or suggests the use of a monomolecular film or a monoatomic film of an alkane thiol.

Claim 64 of the presently claimed invention recites “[a] method for applying a material between a semiconductor device having a surface and a substrate having a surface, said semiconductor device mounted on said substrate, said method comprising: applying a essentially uniform liquid silane-based wetting agent layer having a total thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate; and applying a flowable underfill material between the substrate and the semiconductor device separately from said liquid silane-based wetting agent layer, such that said flowable material contacts said wetting agent layer.”

Appellant asserts that any combination of the Yamada et al. reference, the Schulz et al. reference, the Pluddemann reference and the Hieda et al. reference fails to teach or suggest the claim limitations of independent claim 64 calling for “applying a essentially uniform liquid silane-based wetting agent layer having a total thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate” and “applying a flowable underfill material between the substrate and the semiconductor device separately from said liquid silane-based wetting agent layer, such that said flowable material contacts said wetting agent layer.”

Appellant asserts that the Yamada et al. reference clearly uses a thermo-setting material as an underfill material because the Yamada teaches or suggests thermo-setting resin. (Yamada,

col. 56, lines, 23-61). Contrary to the Examiner's assertion, Yamada does not teach that the "underfill material is not limited to thermosetting material," but rather that the "resin is not limited to bisphenol type epoxy resin." (Cf., October 20, 2006, Office Action, page 9 and Yamada col. 70, lines 8-14 and 62).

Appellant further asserts that the Yamada et al. reference cannot teach or suggest the use of a thermo-plastic underfill because a thermo-plastic underfill would soften with an increase of temperature when the IC chip is being operated so that the thermo-plastic underfill would be unable to compensate for any thermal mismatch between IC chip and the IC carrier thereby making the Yamada et al. invention inoperable due to the thermo-plastic material losing its strength as it is heated thereby allowing the IC chip to separate from the substrate as the bump electrodes 203 fail in shear due to the thermo-plastic material carrying no load. Additionally, thermo-plastic materials have too high viscosity to be used as underfill materials as they are unable to effectively fill the small space between an IC chip mounted on an IC chip carrier using solder balls where the small space is 125 microns or less in height. Further, in contrast to the elements of the presently claimed invention of independent claim 64, the Yamada et al. reference describes the use of a wax layer or resin layer while the Hieda et al. references use an alkane thiol layer.

The Examiner cites the Schultz reference for teaching the use of a thermoplastic underfill material. (October 20, 2006, Office Action, page 9). Appellant asserts that the Schultz reference solely teaches or suggests the use of a thermoplastic material for an encapsulant.

Appellant asserts that both the Schulz et al. reference and the Pluddemann reference teach away from any combination with and modification of the Yamada et al. reference. Yet further, Appellant asserts that one of ordinary skill in the art would not substitute the use of a thermo-plastic for the thermo-setting underfill of Yamada et al. Appellant asserts that one of ordinary skill in the art would not substitute either the thermo-plastic resin of the Schultz et al. reference or the liquid primer composition from the Pluddemann reference to be separately applied to the IC chip and/or IC carrier of the Yamada et al. reference. The substitution of a thermo-plastic resin of Schultz et al. for a thermo-setting resin of Yamada et al. destroys the Yamada et al. invention as it would fail since in operation, the thermoplastic resin of Schultz et al. would allow the device to separate and the bump electrodes 203 to fail in shear due to the

thermo-plastic resin carrying no load. Further, Appellant asserts that the substitution of a liquid primer composition from the Pluddemann reference for a resin of the Yamada et al. reference cannot be the substitution of an equivalent. Appellant asserts that one of ordinary skill in the art would not use the Pluddemann liquid primer composition for use with thermo-setting plastics of Yamada et al.

Appellant asserts that the sole teaching or suggestion for the use of a liquid wetting agent on one of the active surface of said semiconductor device and a portion of said upper surface of said substrate for use with an underfill material is solely the Appellant's disclosure because the cited prior art teaches away from any combination thereof, because if the prior art is combined as suggested in the rejection, the combination clearly destroys the operability of the primary reference and because the cited prior art does not contain any suggestion for any combination thereof. Solely Appellant's disclosure contains any such suggestion as evidenced by the attempt to combine the cited prior art in a rejection which destroys the invention of the Yamada et al. reference.

Therefore, Appellant asserts that any combination of the Yamada et al. reference, the Schultz et al. reference, the Pluddemann reference and the Heida reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 64. Accordingly, the rejection of independent claim 64 should be reversed.

- c. Claims 13, 14, 16-21 and 23-30 stand rejected under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz (U.S. Patent 6,350,840) and Pluddemann (U.S. Patent 4,961,967) and in further combination with Akram (U.S. Patent 5,766,982).

The discussion of Yamada, Schultz and Pluddemann, *supra*, is incorporated herein. Akram is cited for teaching underfill methods and fails to cure the deficiencies of Yamada, Schultz and Pluddemann. Claims 13, 14, 16-21 and 23-30 depend from independent claim 10. The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as

rendering dependent claims 13, 14, 16-21 and 23-30 obvious, cannot serve as a basis for rejection. Accordingly, the rejection of claims 13, 14, 16-21 and 23-30 should be reversed.

- d. Claims 31 and 32 stand rejected under 35 U.S.C. §103(a) as being obvious over Yamada in view of Schultz and Pluddemann as applied to claim 10, and in further combination with Banerji (U.S. Patent 5,203,076).

The discussion of Yamada, Schultz and Pluddemann, *supra*, is incorporated herein. Banerji is cited for teaching vacuum infiltration of underfill material and fails to cure the deficiencies of Yamada, Schultz and Pluddemann. Claims 31 and 32 depend from independent claim 10. The Court of Appeals for the Federal Circuit has stated that “dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.” In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 31 and 32 obvious, cannot serve as a basis for rejection. Accordingly, the rejection of claims 31 and 32 should be reversed.

8) CLAIMS APPENDIX

A copy of claims 1-5, 7-32 and 58-64 is appended hereto as Appendix A.

9) EVIDENCE APPENDIX

There is no evidence appendix.

10) RELATED APPEALS APPENDIX

There is no related appeals appendix.

CONCLUSION

Appellant respectfully submits that claims 1-5, 7-32 and 58-64 are allowable. Appellant respectfully requests that the rejection of claims 58-61 under 35 U.S.C. §102(e) and claims 1-5, 7-32 and 62-64 under 35 U.S.C. § 103(a), be reversed.

Respectfully submitted,



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APPENDIX A

Claims Appendix

Claims 1-5, 7-32 and 58-64

U.S. Patent Application No. 09/544,822

Filed April 6, 2000

1. A method for applying a material between a semiconductor device having a surface and a substrate having a surface, said method comprising:
applying a liquid wetting agent layer to one of said surface of said semiconductor device and said surface of said substrate; and
applying a flowable underfill material between the substrate and the semiconductor device, such that said flowable material contacts said liquid wetting agent layer.
2. The method according to claim 1, wherein said semiconductor device is attached to said substrate.
3. The method of claim 1, wherein said liquid wetting agent layer includes a layer of silane-based material.
4. The method according to claim 1, wherein said applying said liquid wetting agent layer comprises any one of a dispensing method, a brushing method, and a spraying method.
5. The method according to claim 1, wherein said liquid wetting agent layer comprises at least one layer.
7. The method according to claim 1, wherein said liquid wetting agent layer comprises a plurality of layers.

8. The method according to claim 1, wherein said liquid wetting agent layer comprises one of glycidoxypyriltrimethoxysilane and ethyltrimethoxysilane.

9. The method according to claim 1, wherein said applying a liquid wetting agent layer comprises providing a material that to the surface of one of said surface of said semiconductor device and said surface of said substrate for the application of an underfill material.

10. A method for applying a material between a semiconductor device and a substrate, said method comprising:

providing a semiconductor device having an active surface, another surface, a first end, a second end, a first lateral side, and a second lateral side, said first end, said second end, said first lateral side, and said second lateral side forming at least a portion of a periphery of said semiconductor device;

providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall;

applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; and

applying a flowable underfill material between said semiconductor device and said substrate, such that said flowable material contacts said applied liquid wetting agent layer.

11. The method according to claim 10, wherein said flowable material is applied substantially adjacent to at least one end of said semiconductor device.
12. The method according to claim 10, wherein said flowable material substantially fills a gap between said semiconductor device and said substrate.
13. The method according to claim 10, wherein said substrate includes an aperture extending through said substrate.
14. The method according to claim 13, wherein said aperture is located adjacent to said another surface of said semiconductor device.
15. The method according to claim 10, wherein said flowable material is provided substantially adjacent to said at least a portion of the periphery of said semiconductor device to fill a gap between said substrate and said semiconductor device.
16. The method according to claim 10, further comprising:
elevating at least said first side wall of said substrate and said first end of said semiconductor device.

17. The method according to claim 16, wherein said elevating said first side wall of said substrate comprises placing said substrate on a support structure and elevating at least one portion of said support structure.

18. The method according to claim 16, further comprising:
providing a dam on the substrate adjacent to at least one of said first end, said second end, said first lateral side and said second lateral side of said semiconductor device.

19. The method according to claim 18, wherein said dam extends to substantially between said semiconductor device and said substrate.

20. The method of claim 10, further comprising:
vibrating one of said semiconductor device and said substrate.

21. The method according to claim 20, wherein said vibrating one of said semiconductor device and said substrate comprises placing said substrate on a support structure and vibrating said support structure.

22. The method according to claim 10, wherein said applying said flowable material comprises:
providing said flowable material substantially adjacent said first end of said semiconductor

device for filling between said substrate and said semiconductor device by one or more forces acting upon said flowable material.

23. The method according to claim 10, wherein said substrate includes at least one aperture extending through said substrate and substantially located adjacent to said another surface of said semiconductor device.

24. The method according to claim 23, wherein said flowable material is provided through said at least one aperture of said substrate substantially filling a gap between said substrate and said semiconductor device.

25. The method according to claim 18, wherein said applying said flowable material comprises:
providing said flowable material substantially adjacent to said first end of said semiconductor device for filling a gap between said substrate and said semiconductor device.

26. The method according to claim 18, wherein said applying said flowable material comprises:
providing said flowable material substantially adjacent to said first end and one of said first lateral side and said second lateral side of said semiconductor device for filling a gap between said substrate and said semiconductor device.

27. The method according to claim 18, wherein said substrate includes at least one aperture extending therethrough and substantially located adjacent to said another surface of said semiconductor device.

28. The method according to claim 27, wherein said flowable material is provided through said at least one aperture.

29. The method according to claim 28, wherein said flowable material is provided from below said substrate.

30. The method according to claim 28, wherein said flowable material is provided through said at least one aperture contacting at least a portion of said another surface of said semiconductor device.

31. The method according to claim 10, wherein said applying said flowable material between said semiconductor device and said substrate further comprises placing said semiconductor device and said substrate in a chamber, said chamber having an atmosphere therein having a variable pressure.

32. The method according to claim 31, further comprising:
varying the pressure of said atmosphere in said chamber for said flowable material substantially filling a gap between said semiconductor device and said substrate.

58. A method for attaching a semiconductor assembly, said method comprising:
providing a semiconductor device having an active surface;
providing a substrate having an upper surface;
applying a liquid wetting agent layer to one of said active surface of said semiconductor device
and said upper surface of said substrate;
connecting said semiconductor device to said substrate so that said active surface of said
semiconductor device faces said upper surface of said substrate; and
applying a flowable underfill material between the substrate and the semiconductor device, such
that said flowable underfill material contacts said applied wetting agent layer.

59. The method according to claim 58, wherein applying said wetting agent layer
comprises any one of a dispensing method, a brushing method, and a spraying method.

60. The method according to claim 58, wherein said wetting agent layer comprises at
least one layer.

61. The method according to claim 58, wherein said wetting agent layer comprises a
silane-based material.

62. A method for attaching a semiconductor assembly, said method comprising:
providing a semiconductor device having an active surface, a first end, a second end, a first
lateral side end and a second lateral side end;

providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall;

applying a silane-based material layer to one of a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate;

connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and

applying a flowable underfill material between said semiconductor device and said substrate, such that said flowable underfill material contacts said applied silane-based material layer.

63. The method according to claim 61, wherein said wetting agent layer comprises one of glycidoxypyltrimethoxysilane and ethyltrimethoxysilane.

64. A method for applying a material between a semiconductor device having a surface and a substrate having a surface, said semiconductor device mounted on said substrate, said method comprising:

applying a essentially uniform liquid silane-based wetting agent layer having a total thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate; and

applying a flowable underfill material between the substrate and the semiconductor device separately from said liquid silane-based wetting agent layer, such that said flowable material contacts said wetting agent layer.